Numonyx™ StrataFlash® Wireless Memory (L30) to Intel® PXA255 Processor Design Guide

Application Note - 805

November 2007
Contents

1.0 Introduction .............................................................................................................. 1
   1.1 L30 Device ......................................................................................................... 1
   1.2 Intel® PXA250 Applications Processor .......................................................... 1

2.0 Hardware Interfaces ................................................................................................. 2
   2.1 Flash Memory Interface ................................................................................... 2
   2.2 Processor Memory Interface ........................................................................... 3

3.0 Interface Considerations ......................................................................................... 5
   3.1 Hardware Connections ..................................................................................... 5
   3.2 Reset Operation ............................................................................................... 6

4.0 Register Settings ..................................................................................................... 7
   4.1 Flash Memory Register Settings ...................................................................... 7
   4.2 Processor Register Settings ............................................................................ 8

5.0 Bus Operation and Timings ....................................................................................... 9
   5.1 Asynchronous Single Reads ........................................................................... 9
   5.2 Asynchronous Page-Mode Reads ................................................................... 10
   5.3 Synchronous Burst-Mode Reads ................................................................... 11
   5.4 Asynchronous Writes .................................................................................... 12

6.0 Summary ................................................................................................................ 13

A Additional Information ............................................................................................ 13
## Contents

<table>
<thead>
<tr>
<th>Date of Revision</th>
<th>Version</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>12/10/02</td>
<td>-001</td>
<td>Initial Release</td>
</tr>
<tr>
<td>November 2007</td>
<td>02</td>
<td>Applied Numonyx branding.</td>
</tr>
</tbody>
</table>
1.0 Introduction

This application note covers interfacing the Numonyx™ StrataFlash® Wireless Flash Memory (L30) device to the Intel* PXA250 Applications Processor, and discusses some general concepts involved when interfacing to the integrated features and control signals of the L30 device.

This document was written based on information available at the time on the L30 device and the Numonyx PXA250 Applications Processor. It is assumed that the reader is already familiar with these devices and has a working knowledge of them.

Any changes in specifications to either device since then may not be reflected in this document. Refer to the appropriate documents or sales personnel for the most current information before finalizing any design.

1.1 L30 Device

The Numonyx™ StrataFlash® Wireless Flash Memory (L30) device combines reliable and proven two-bit-per-cell technology with multi-partition read-while-write (RWW) and read-while-erase (RWE) dual operation. It provides high-performance asynchronous-page and synchronous-burst read modes using 1.8 volt low-voltage, multi-level cell (MLC) technology. It is a 1.8 volt core device (V\text{CC}) with a 3-volt I/O (V\text{CCQ}). A 1.8 volt I/O version is also available.

The multi-partition architecture of the L30 device enables background programming or erasing to occur in one partition, while code execution or data reads take place in another partition, simultaneously. These devices are ideal for mainstream applications requiring large storage space for both code and data. Advanced system designs can benefit from the dual-operation architecture by enabling two processors to interleave code operations while program or erase operations take place in the background. 8-Mbit and 16-Mbit partition sizes allow system designers to choose the size of the code and data segments best suited for the particular system design.

1.2 Intel* PXA250 Applications Processor

The PXA250 applications processor is an Intel XScale™ core-based microprocessor. Intel XScale is 32-bit RISC micro architecture, that is ARM architecture compliant, based on architecture by Advanced RISC Machines (ARM*). Designed for high performance at low power, the PXA250 applications processor incorporates a comprehensive set of system and peripheral functions enabling it to be used in a variety of portable handheld and handset devices. A rich set of serial devices and general system resources provide enough compute and connectivity capability for applications such as palm-size PCs, Smartphones, and wireless PC Companions.

The PXA250 applications processor contains a 32-KByte instruction cache and a 32-KByte data cache, using a 256-bit line-fill buffer. The on-chip memory controller is based on a Unified Memory Architecture wherein all external memory devices share a common address and data bus. The memory controller consists of four main control units for interfacing with dynamic memory (SDRAM), static memory (ROM, SRAM, Flash), PCMCIA, and companion chips. External memory is viewed as a linear collection of bytes numbered upwards from 0.
2.0 Hardware Interfaces

This section describes the hardware interface signals between the L30 device and the Intel PXA250 Applications Processor. This document assumes that all other device signals and power supplies are connected in such a way as to ensure proper device operation.

2.1 Flash Memory Interface

The L30 device integrates several hardware features that enable it to be used with a range of burst processors such as the Intel PXA250 Applications Processor. These features include:

- Address Latch (ADV#)
- Read Configuration Register (RCR)
- Internal burst-address generator
- Burst Suspend

The address latch (ADV#) is used to latch the address during read operations. CPUs that employ a multiplexed address/data bus can utilize the internal latch to demultiplex the address/data bus. ASICs can also use the latch to reduce pin count while improving performance.

The Read Configuration Register (RCR) is used to configure the flash memory component to specific CPU characteristics. These include read mode (synchronous or asynchronous), burst length (4-, 8-, 16-, or Continuous words), burst latency, valid clock edge and WAIT configuration.

The RCR settings also inform the internal burst-address generator how to generate addresses during synchronous-burst reads. Generating addresses internally eliminates the memory’s dependence on the CPU for the next address during a burst read, improving system read performance.

Burst suspend enables the system to access another device during a burst-read sequence. The system processor can resume the burst sequence at a later time.

The hardware interface of the L30 device has the following signals:


D[15:0] DATA I/O: Inputs during write operations, outputs during read operations, and High-Z (float) when CE# or OE# is deasserted.

CE#CHIP ENABLE: Low-true input. CE#-low enables the device. CE#-high disables the device, placing it in standby mode. CE#-high places data and WAIT signals at High-Z.

OE#OUTPUT ENABLE: Low-true input. OE#-low enables the output buffers. OE#-high disables data output buffers placing all data outputs at High-Z.

WE#WRITE ENABLE: Low-true input. WE#-low enables the write buffers. Address and data are latched on the rising edge of WE# or the rising edge of CE# while is WE# low, whichever occurs first.

WP#WRITE PROTECT: Low-true input. WP#-low enables the lock-down mechanism. Blocks configured for lock-down cannot be unlocked with the Unlock-Block command. WP#-high overrides the lock-down mechanism enabling blocks to be programmed or erased.
CLKCLOCK: CLK synchronizes the device to the system bus clock and increments the internal address generator in synchronous-burst read mode. In synchronous-burst read mode, the initial address is latched on the rising edge of ADV# or the next valid clock edge when ADV# is low, whichever occurs first.

ADV#ADDRESS VALID: Low-true input. In synchronous-burst read mode, the initial address is latched on the rising edge of ADV# or the next valid clock edge when ADV# is low, whichever occurs first.

WAITWAIT: Output; configurable for high-true or low-true. Indicates invalid data in synchronous-burst read mode. WAIT is High-Z whenever CE# is deasserted (not gated by OE#). WAIT is not used in this design example.

RST#RESET: Low-true input. RST# resets internal automation and inhibits write operations. RST#-high enables normal operation.

VCCCore Power Supply. Core source voltage (1.7 V to 2.0 V).

VCCQI/O Power Supply. Output driver source voltage (2.2 V to 3.3 V); connect to the same supply as VCCN on the PXA250.

2.2 Processor Memory Interface

The external memory interface of the PXA250 applications processor supports a variety of memory types including SDRAM, page and burst mode flash memory, synchronous masked ROM (SMROM), page-mode ROM, SRAM, SRAM-like Variable Latency I/O (VLIO) memory, PCMCIA expansion memory, and compact flash (see Figure 1). Memory type and timing parameters are programmable through the PXA250 applications processor’s memory controller configuration registers.

The external memory controller also supports the presence of an alternate bus master on the SDRAM memory bus. The alternate master is given control of the bus through a bus request/ bus grant hardware handshake. Refer to the Intel PXA250/ PXA210 Applications Processor Developer’s Manual (order number 278522) for details.
The PXA250 applications processor uses the following external memory interface signals in this example design:

MA[25:0] Memory Address Bus. The memory address bus transfers address information between the processor and external memory.

MD[31:0] Memory Data bus. The memory data bus carries data between the processor and external memory.

SDCLK[2:0] Synchronous Memory Clocks. Used to synchronize data transfers between the processor and the selected external memory. SDCLK0 is used for synchronous transfers from Static Banks 0-3. SDCLK1 and SDCLK2 are used for SDRAM partitions.

nSDCASSDRAM Column Address Strobe. Active-low output, nSDCAS is used to latch the initial-access address during burst reads from synchronous flash memory.
nCS[5:0] Static Memory Chip Selects. Active-low outputs, the chip selects are individually programmable through the memory configuration registers. nCS0 is initialized at reset for boot-ROM selection.

nOEO Output Enable. Active-low output, nOE is asserted during memory reads to enable the data bus drivers of the selected external memory device.

nWE Write Enable. Active-low output, nWE is asserted during write operations to external memory devices.

nRESET Hard reset. Low-true input, used to start the processor from a known state and address. On startup, nRESET must remain low until the power supply and internal oscillator has stabilized.

nRESET_OUT Reset out. Low-true output, asserted when nRESET is asserted, and deasserted after nRESET is deasserted, but before the first instruction fetch. nRESET_OUT is also asserted for “soft” reset events such as sleep, watchdog reset, and GPIO reset.

RDY READY. High-true input, Variable Latency I/O data ready. Not used in this design example.

VCCN Positive supply for the external memory bus I/O. The VCCN voltage range is 2.375 V to 3.6 V; connect to the same supply as VCCQ on the 28F256L30.

3.0 Interface Considerations

This design example uses two 28F256L30B90 flash memory devices interfaced with the PXA250 applications processor on a 32-bit wide data bus. It is assumed that the flash memory is mapped into the bootROM space of the PXA250 applications processor. When the PXA250 applications processor comes out of reset, it begins fetching and executing instructions at address 0x0000, which corresponds to nCS0.

The interface timings reflect a MEMCLK frequency of 100MHz, with an SDCLK0 frequency of 50 MHz. Other bus speeds and memory sizes can be substituted by changing the appropriate processor and flash memory register settings described in the following sections.

This sample interface design does not include all information regarding system initialization, interrupt control, exception handling, or other peripheral device operations. External device signals/pins should be asserted or negated as necessary for desired device operation. Also, proper power supply voltages must be applied in accordance with the latest datasheet information. Be sure to read all applicable documentation (e.g., datasheets, user manuals, specification updates) before attempting this interface.

3.1 Hardware Connections

Figure 2 shows the hardware connections between the 28F256L30 flash memories and the PXA250 applications processor. This design example uses chip select nCS0; however, any of the other static memory chip selects can be used instead by configuring the appropriate chip select registers. Also note that only nCS[3:0] support synchronous-burst reads.

Upon start-up (reset), the PXA250 applications processor samples the BOOT_SEL[2:0] input pins to determine the type of boot memory. Since the 28F256L30 flash memory powers up in asynchronous read mode, BOOTSEL[2:0] is shown configured for asynchronous 32-bit ROM.
Address bit A0 on each of the flash memories is the least significant word (x16) address bit. With two devices configured for x32 operation, the least significant double-word (x32) address bit from the PXA250 applications processor is A2, and is connected to A0 on each of the flash memories. The rest of the address bits are connected sequentially up to the most significant address bit.

Note: For x16 operation with a single flash device, A1 from the PXA250 would be connected to A0 on the flash memory, and BOOT_SEL0 would be pulled up to configure the processor for x16 operation at boot-up.

For burst read operations, the 28F256L30 uses SDCLK0 for the burst clock. If only asynchronous read operations are to be performed, it is recommended that the CLK input of the 28F256L30 be tied to a valid VIH level.

### 3.2 Reset Operation

The PXA250 nRESET_OUT signal must be connected to the RST# input on the 28F256L30 for Hardware reset, Watchdog reset and sleep mode to work properly. GPIO reset, however, does not reset the contents of the PXA250 Memory Controller registers. If GPIO reset operation is required, a state machine is necessary between nRESET_OUT, GPIO[1] and RST# to ensure that RST# is asserted during a hardware reset.
reset, Watchdog reset and sleep mode, but not asserted during GPIO resets (see Figure 3). GPIO_a is an unused GPIO that is driven low by software during the initialization sequence and left high during normal operation.

**Figure 3: Reset State Machine**

<table>
<thead>
<tr>
<th>GPIO[1]</th>
<th>nSet Q</th>
<th>nRESET_OUT</th>
<th>nRESET</th>
<th>RST#</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO_a</td>
<td>nClear</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

If Watchdog reset is not necessary, a secondary GPIO can control nRESET_OUT using the equation:

\[ \text{RST#} = \text{nRESET} \& (\text{nRESET}_\text{OUT} + \text{GPIO}_a) \]

This allows sleep mode entry to reset the 28F256L30 while keeping it in synchronous read mode during a GPIO reset (see Figure 4). GPIO_a is an unused GPIO that is kept high during normal operation and driven low before entering sleep mode.

**Figure 4: Reset Logic - No Watchdog Reset**

<table>
<thead>
<tr>
<th>GPIO_a</th>
<th>nRESET_OUT</th>
<th>nRESET</th>
<th>RST#</th>
</tr>
</thead>
</table>

4.0 Register Settings

After a system reset, processor and flash memory registers must be programmed with appropriate values to enable the processor to utilize the synchronous burst-mode read feature of the 28F256L30. The following sections describe the affected registers and their settings.

4.1 Flash Memory Register Settings

The default read mode of the 28F256L30 is asynchronous read array mode featuring a 4-word page buffer. To enable synchronous burst mode, the Read Configuration Register (RCR) of both flash memories must be programmed. The default value of the RCR is 0xFFFF. For this example, programming each RCR with a value of 0x25C2 configures the flash devices for synchronous burst reads as follows:

- Read Mode (RCR15) = 0b0 (Synchronous Burst Mode)
- Reserved (RCR14) = 0b0
- Latency Count (RCR[13:11]) = 0b100 (Code 4)

**Note:** The latency count is calculated for a 50 MHz burst clock. See the 28F256L30 datasheet for details.

- WAIT Polarity (RCR10) = 0b1 (WAIT is high-true; default; not used)
- Data Hold (RCR9) = 0b0 (hold data for one clock)
- WAIT Delay (RCR8) = 0b1 (WAIT deasserted before valid data; default; not used)
- Burst Sequence (RCR7) = 0b1 (linear burst sequence; default)
- Clock Edge (RCR6) = 0b1 (rising edge; default)
• Reserved (RCR[5:4]) = 0b00
• Burst Wrap (RCR3) = 0b0 (Burst accesses wrap within the burst length set by RCR[2:0])
• Burst Length (RCR[2:0]) = 0b010 (8-word burst)

To program the RCR, the desired register value is driven onto the address bus by the processor when issuing the Program RCR setup command (0x60) and the confirm command (0x03). The "offset" of the address connections between the processor and the flash devices (see Figure 2, "Hardware Connections" on page 6) requires the register value to be shifted two places to the left. Therefore, the RCR value of 0x1DC2 becomes 0x7708 for this x32 example design. This is the address used when issuing the Program RCR setup and confirm commands to the flash devices. Also, because the bus interface is x32, the data values are 0x0060.0060 for the setup command and 0x0003.0003 for the confirm command.

4.2 Processor Register Settings

The PXA250 applications processor contains registers used to configure the operation of the external memory interface. The settings for the Core Clock Configuration Register (CCCR), SDRAM Refresh Control Register (MDREFR), Synchronous Static Memory Control Register (SXCNFG), and Static Memory Control Register (MSC[2:0]) are described in the following sections. Register bit fields that affect the external memory interface operations with the 28F256L30 are discussed; all other bit fields should be programmed as necessary to ensure proper operation.

4.2.1 Core Clock Configuration Register (CCCR)

The PXA250 applications processor contains a Clocks Manager used to manage its multiple clock sources and power saving functions. The Core Clock Configuration Register (CCCR) is used to set the memory controller’s clock frequency (MEMCLK). For this design example, a clock multiplier setting of 27 (CCCR:L[4:0] = 0b00001) is used to produce a MEMCLK frequency of 99.53 MHz from a 3.6864 MHz crystal oscillator source. The 'M' and 'N' fields of the CCCR should be programmed for desired core clock operation.

4.2.2 SDRAM Refresh Control Register (MDREFR)

MDREFR provides control of SDCLK0 and its enable pin, SDCKE0. The K0RUN bit (MDREFR13) must be set to enable SDCLK0, while the E0PIN bit (MDREFR12) can be optionally set to enable external pin control of SDCLK0. Since the maximum input clock frequency of the 28F256L30 is 66 MHz, the K0DB2 bit (MDREFR14) must be set to configure SDCLK0 to run at one-half the MEMCLK frequency, or approximately 50 MHz.

4.2.3 Synchronous Static Memory Configuration Register (SXCNFG)

The PXA250 applications processor supports synchronous-burst flash memory such as the 28F256L30. The SXCNFG register is used to configure nCS[3:0] in pairs for either synchronous masked ROM (SMROM), SDRAM-like synchronous flash, or non-SDRAM timing synchronous flash. SXCNFG[15:0] configures chip selects nCS[1:0], while SXCNFG[31:16] configures chip selects nCS[3:2].

Programming SXCNFG[15:0] with 0x60F1 configures nCS0 (Static Bank 0) for synchronous burst-mode reads with the 28F256L30 flash memories as follows:
• Reserved (SXCNFG15) = 0b0
• SXLATCH0 (SXCNFG[14]) = 0b1 (latch data with SDCLK0)
• SXTP0 (SXCNFG[13:12]) = 0b10 (non-SDRAM timing synchronous flash)
• SXCA0 (SXCNF[11:10]) = 0b00 (not used)
• SXRA0 (SXCNF[9:8]) = 0b00 (not used)
• SXRL0 (SXCNF[7:5]) = 0b111 (not used)
• SXCL0 (SXCNF[4:2]) = 0b100 (CAS latency; five SDCLKs)
• SXEN0 (SXCNF[1:0]) = 0b01 (Static Bank 0 enabled for SX memory)

4.2.4 Asynchronous Static Memory Control Registers (MSC[2:0])

MSC[2:0] are the registers used to configure static memory chip selects nCS[5:0] for asynchronous memory accesses. Each of the three MSC registers contain two identical 16-bit configuration fields- one for each of its corresponding static memory chip selects.

**Note:** All timing fields are specified in MEMCLK cycles.

If any of the nCS[3:0] static memory banks is configured for synchronous static memory operation via SXCNF:SXENx, the corresponding half-word of MSC[1:0] is ignored. However, the data-width field, RBWx, within the affected half-word is still used. Also, for non-SDRAM timing synchronous flash (SXCNF:SXTPx = 0b10), the MSCx register values are still used for the asynchronous flash write timings.

The MSCx:RDFx and MSCx:RDNx fields configure the delay timings (wait states) for the initial-access and subsequent page-accesses, respectively. The MSCx:RTx field configures the type of memory used. The 28F256L30 supports 4-word asynchronous page-mode reads.

Programming MCS0[15:0] with 0x2282 configures nCS0 for burst-of-four asynchronous page-mode reads with the 28F256L30 as follows:

• RBUFF0 (MSC0[15]) = 0b0 (Slower device - Return Data Buffer)
• RRR0 (MSC0[14:12]) = 0b010 (read recovery: 30 ns)
• RDN0 (MSC0[11:8]) = 0x0010 (ROM delay - next access: 30 ns)
• RDF0 (MSC0[7:4]) = 0b1000 (ROM delay - first access: 100 ns)
• RBW0 (MSC0[3]) = 0b0 (data bus width: 32 bits)
• RT0 (MSC0[2:0]) = 0b010 (memory type: burst-of-four flash w/ non-burst writes)

5.0 Bus Operation and Timings

For the following discussions, consult the appropriate PXA250 applications processor and 28F256L30 flash memory documents for specific timing information of the individual components presented in this design example. Flash memory timings start with R (read) or W (write).

5.1 Asynchronous Single Reads

The PXA250 applications processor registers default to settings upon reset allowing it to access the slowest ROMs available. In this example, the BOOT_SEL[2:0] pins are tied low (see Figure 2, “Hardware Connections” on page 6). This configures the PXA250 applications processor for an asynchronous 32-bit ROM with the maximum number of wait states at startup.
The 28F256L30 defaults to asynchronous read-array mode at startup, and all of the burst-read configuration bits of its Read Configuration Register are ignored. Figure 5 shows the bus timings for an initial asynchronous single read following a reset. Note that R5 must be satisfied before reading from the flash memories.

**Figure 5: Async Single-Read Bus Timing**

---

**5.2 Asynchronous Page-Mode Reads**

The 28F256L30 defaults to Read Array upon reset. Also, the default operating mode is Asynchronous Page mode. When reads occur, array data is copied into a high-speed page buffer. The page-buffer size of each 28F256L30 is four 16-bit words. In this design example, the two 28F256L30 devices yield a total page-buffer size of four 32-bit DWords (x32).

The PXA250 applications processor supports burst-of-four or burst-of-eight asynchronous reads. The processor’s low-order memory address lines (MA[3:2]) control accesses to the data within the flash page buffer- no additional flash commands are necessary for asynchronous page-mode operation.
5.3 Synchronous Burst-Mode Reads

In synchronous read mode, the PXA250 only supports burst-of-eight reads. Figure 7 shows the bus timings for 8-word synchronous burst reads.

At the start of a synchronous-burst read cycle, the PXA250 drives the address onto MA[25:2], asserts nCS0 one MEMCLK later, then asserts nSDCAS one MEMCLK after that. The rising edge of SDCLK0 with nSDCAS (ADV#) low causes the 28F256L30 to latch the initial address. nSDCAS remains low for three MEMCLK periods, then deasserts. In this design example, it is important to note that SDCLK0 is running at one-half the frequency of MEMCLK.

The PXA250 asserts OE# two SDCLK0 periods before the end of the CAS delay. For this design example with a CAS latency of four clocks, OE# asserts after two SDCLK0 periods.

After the initial-access latency period has elapsed, the PXA250 applications processor samples the read data on the rising edge of SDCLK0. Subsequent burst reads are sampled on the rising edges of SDCLK0 with zero wait states.
5.4 Asynchronous Writes

The value programmed into MSC0:RDF0 determines the number of MEMCLK cycles that nWE (WE#) is asserted for page-mode flash (RT0 = 0b010 or 0b011). MSC0:RDN0 determines the nWE (WE#) assert time for non-page-mode flash (RT0 = 0b000).

In this design example using page-mode, RDF0 can be programmed with a minimum of five MEMCLK cycles. This register setting would cause nWE to be asserted for six MEMCLK cycles, or 50 ns, satisfying the flash devices' WE#-low specification, W3. The flash devices sample the write address and write data on the rising edge of nWE or nCE, which ever occurs first. Figure 8 shows the bus timings for an asynchronous write to the 28F256L30.
6.0 **Summary**

The L30 device is the latest generation of the Numonyx StrataFlash® memory device featuring flexible, multi-partition, dual operation. It provides high-performance asynchronous page-mode reads and synchronous burst-mode reads using 1.8 volt low-voltage, multi-level cell (MLC) technology. The multi-partition architecture enables background programming or erasing to occur in one partition while code execution or data reads take place in another partition.

The flexible interface of the L30 device gives the designer a simple “glueless” interface with processors such as the PXA250 which helps to reduce power consumption, decrease system costs and increase overall system reliability by eliminating the need for additional interface components.

The L30 device is available in several densities for increased flexibility, and an excellent option for both code and data applications where high density and low cost is required.

**Appendix A Additional Information**

<table>
<thead>
<tr>
<th>Order Number</th>
<th>Document/Tool</th>
</tr>
</thead>
<tbody>
<tr>
<td>251903</td>
<td>Numonyx™ StrataFlash® Wireless Flash Memory (L30) Datasheet</td>
</tr>
<tr>
<td>292286</td>
<td>AP-738 Reduce Manufacturing Costs with Numonyx™ Flash Memory Enhanced Factory Programming</td>
</tr>
<tr>
<td>278522</td>
<td>Intel PXA250/ PXA210 Application Processors Developer’s Manual</td>
</tr>
<tr>
<td>278523</td>
<td>Intel PXA250/ PXA210 Application Processors Design Guide</td>
</tr>
<tr>
<td>278524</td>
<td>Intel PXA250/ PXA210 Application Processors Electrical, Mechanical, and Thermal Specification</td>
</tr>
</tbody>
</table>

**Notes:**
1. Please call the Numonyx Literature Center at (800) 548-4725 to request Numonyx documentation. International customers should contact their local Numonyx or distribution sales office.